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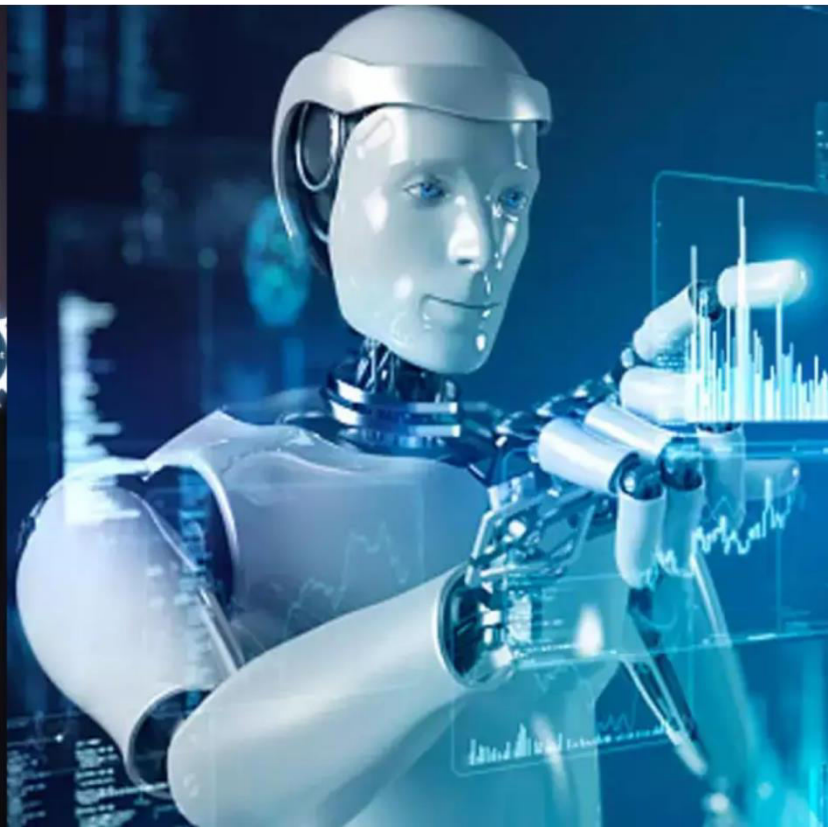

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Fan-Out Analysis and Logical Effort Characterisation of CMOS Inverters in UMC 65nm Technology

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ABSTRACT: This paper presents a rigorous fan-out analysis and logical effort characterisation of CMOS inverters implemented in UMC 65nm technology using Cadence Virtuoso. Fan-out configurations from FO1 to FO8 are systematically evaluated, measuring rising (t_PLH) and falling (t_PHL) propagation delays at the 50% voltage threshold. Detailed analytical derivations using the first-order RC delay model, logical effort theory, and Elmore delay estimation are presented and validated against simulation results. The impact of interconnect geometry on propagation delay is investigated through a post-layout long-wire experiment comparing close and wide routing configurations with full parasitic extraction (PEX). Results confirm that propagation delay scales sub-linearly with fan-out, with only 2.66x increase for an 8x load increase, validating logical effort theory. The parasitic delay component is extracted and quantified. The wide wire configuration achieves a 27% delay reduction, confirming that interconnect resistance is the dominant delay factor in 65nm technology. All results are compared against theoretical predictions, demonstrating strong correlation between analytical models and simulation.

KEYWORDS: Fan-out, logical effort, propagation delay, CMOS inverter, UMC 65nm, wire delay, parasitic extraction, Cadence Virtuoso, electrical effort, Elmore delay, RC delay model, interconnect resistance.

I. INTRODUCTION

The performance of digital integrated circuits is fundamentally governed by the propagation delay of logic gates. As CMOS technology scales into the deep submicron regime, two increasingly significant sources of delay emerge: intrinsic gate delay due to transistor switching characteristics, and extrinsic delay due to interconnect parasitics and fan-out loading [1][7].

Fan-out — defined as the number of identical gate inputs driven by a single output — directly determines the capacitive load seen by the driving gate. In classical first-order models, propagation delay increases linearly with fan-out. However, in nanoscale technologies such as UMC 65nm, non-ideal effects including velocity saturation, mobility degradation, and parasitic capacitances cause significant deviation from ideal linear scaling [7].

Logical effort theory, introduced by Sutherland, Sproull, and Harris [3], provides a powerful and technology-independent framework for analysing delay in terms of logical effort (g), electrical effort (h), and parasitic delay (p). This framework predicts that total delay scales as $d = gh + p$, where the constant parasitic term p prevents purely proportional delay scaling with load.

Furthermore, interconnect delay has become comparable to or exceeding gate delay in advanced technology nodes. The resistance and capacitance of metal routing paths introduce additional signal propagation delays that must be accurately modelled through post-layout parasitic extraction [2].

This paper presents a systematic and analytically rigorous fan-out characterisation of CMOS inverters in UMC 65nm technology [4], covering FO1 through FO8. Theoretical predictions from RC delay models, logical effort, and Elmore delay analysis [9] are derived and compared against Cadence Virtuoso simulation results. A long-wire delay experiment is conducted at post-layout level to quantify interconnect geometry effects. The delay scaling behaviour observed is also consistent with findings reported by Horowitz [8] for MOS timing models.

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II. THEORETICAL BACKGROUND

A. First-Order RC Propagation Delay Model

The propagation delay of a CMOS gate is determined by the time required to charge or discharge the output load capacitance through the effective on-resistance of the conducting transistor network. The first-order RC delay approximation gives [1]:

$t_{pd} \approx 0.69 \times R_{eq} \times C_L$ ...(1)

where R_{eq} is the effective channel resistance of the conducting transistor and C_L is the total output load capacitance. The factor 0.69 = ln(2) arises from the exponential charging characteristic of an RC circuit to the 50% threshold.

The total load capacitance consists of three components:

$C_L = C_{gate} + C_{diffusion} + C_{wire}$ ...(2)

where C_{gate} is the gate capacitance of the driven inverter inputs, $C_{diffusion}$ is the drain diffusion capacitance of the driving inverter, and C_{wire} is the parasitic wire capacitance. For a fan-out of n identical inverters:

$C_L = n \times C_{gate} + C_{diffusion} + C_{wire}$ ...(3)

The average propagation delay is defined as:

$t_{pd} = (t_{PLH} + t_{PHL}) / 2$ ...(4)

where t_{PLH} is the low-to-high output transition delay and t_{PHL} is the high-to-low output transition delay, both measured at the 50% voltage threshold.

B. Effective Resistance Model

The effective resistance R_{eq} of a MOSFET operating in saturation can be approximated as [1]:

$R_{eq} = V_{DD} / (2 \times I_{DSAT})$ ...(5)

where I_{DSAT} is the drain saturation current. For NMOS and PMOS devices respectively:

$R_n = V_{DD} / (2 \times I_{DSAT,n})$ and $R_p = V_{DD} / (2 \times I_{DSAT,p})$ ...(6)

The rising delay (t_{PLH}) is governed by the PMOS pull-up resistance R_p, while the falling delay (t_{PHL}) is governed by the NMOS pull-down resistance R_n:

$t_{PLH} \approx 0.69 \times R_p \times C_L$ and $t_{PHL} \approx 0.69 \times R_n \times C_L$ ...(7)

In the UMC 65nm inverter under study, the transistor dimensions are PMOS: W = 560 nm, L = 60 nm and NMOS: W = 350 nm, L = 60 nm, with a width ratio Wp/Wn ≈ 1.6 selected to partially compensate for lower hole mobility and achieve near-symmetric switching.

C. Logical Effort Theory

Logical effort provides a technology-independent method for comparing delay across different logic gate topologies [3]. The normalised delay d of a gate is:

$d = g \times h + p$ ...(8)

where g is the logical effort (ratio of input capacitance to that of a reference inverter with equal drive strength), h is the electrical effort defined as:

$h = C_{out} / C_{in}$ ...(9)

and p is the parasitic delay representing the intrinsic delay with no external load. For a simple CMOS inverter, g = 1, giving:

$d = h + p$ ...(10)

The absolute delay is obtained by multiplying the normalised delay by the process delay parameter tau (τ):

$t_{pd} = \tau \times d = \tau \times (h + p)$ ...(11)

Since p is constant and independent of fan-out, total delay does not scale linearly with load. As $h = n \times C_{gate} / C_{in}$ increases with fan-out n, the parasitic delay p creates a fixed offset that progressively diminishes the ratio of delay increase to load increase. This is the fundamental reason why delay scales sub-linearly with fan-out.

D. Elmore Delay Model for RC Networks

For distributed RC networks such as interconnect wires, the Elmore delay model provides a more accurate first-order estimate than the lumped RC model [2]:

$t_D = \sum_i (R_i \times C_{i,downstream})$ ...(12)

where R_i is the resistance of each segment and $C_{i,downstream}$ is the total downstream capacitance from that node. For a uniform wire of length L, width W, resistance per unit length r, and capacitance per unit length c:

$R_{wire} = r \times L / W$ and $C_{wire} = c \times W \times L$ ...(13)

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The Elmore delay through the wire becomes:
$t\_wire \approx 0.38 \times R\_wire \times C\_wire = 0.38 \times r \times c \times L^2$ ...(14)
Note that wire delay scales as the square of length L, making long interconnects increasingly problematic in scaled technologies. Increasing wire width W reduces R_wire proportionally while C_wire increases only gradually, resulting in a net delay reduction.

E. Parasitic Delay Extraction from Measurements
From the logical effort model, the parasitic delay p can be extracted from measured data by fitting a linear trend to the delay versus fan-out relationship. Rearranging equation (11):
$t\_pd / tau = n + p$ ...(15)
Plotting t_pd against fan-out n gives a straight line with slope tau (process delay) and y-intercept tau × p. The parasitic delay p can therefore be extracted from the intercept of the linear fit to the measured FO1-FO8 delay data.

III. FAN-OUT = 1 (FO1) BASELINE ANALYSIS

A. Experimental Configuration and Setup
The FO1 configuration consists of a single CMOS inverter driving one identical inverter load, representing the reference condition where C_L = C_gate. This baseline measurement establishes the intrinsic gate delay and provides the reference point for all comparative fan-out analysis.

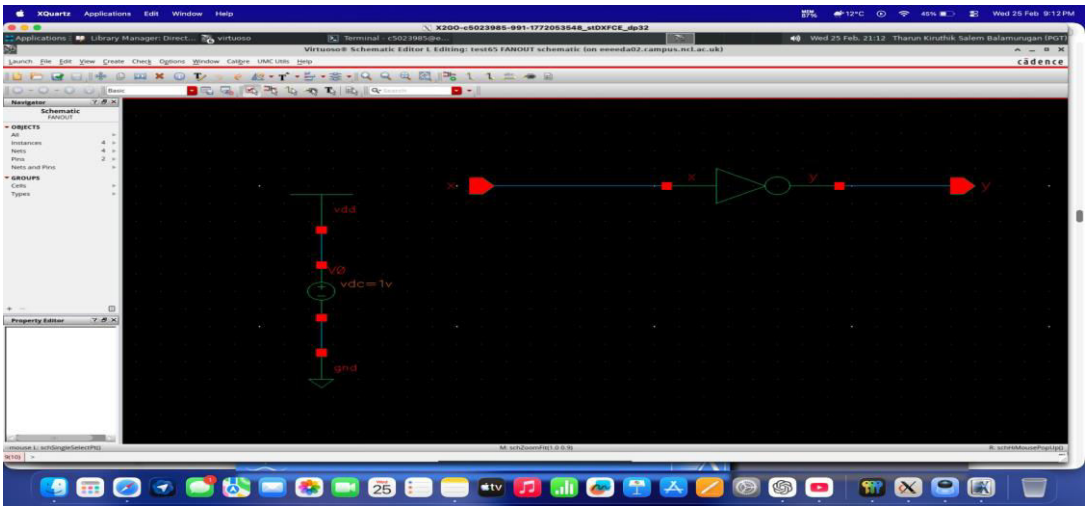

Fig. 1. FO1 test configuration: driving inverter with one identical inverter load at 1V supply in UMC 65nm.

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B. Measured Results and Analytical Verification

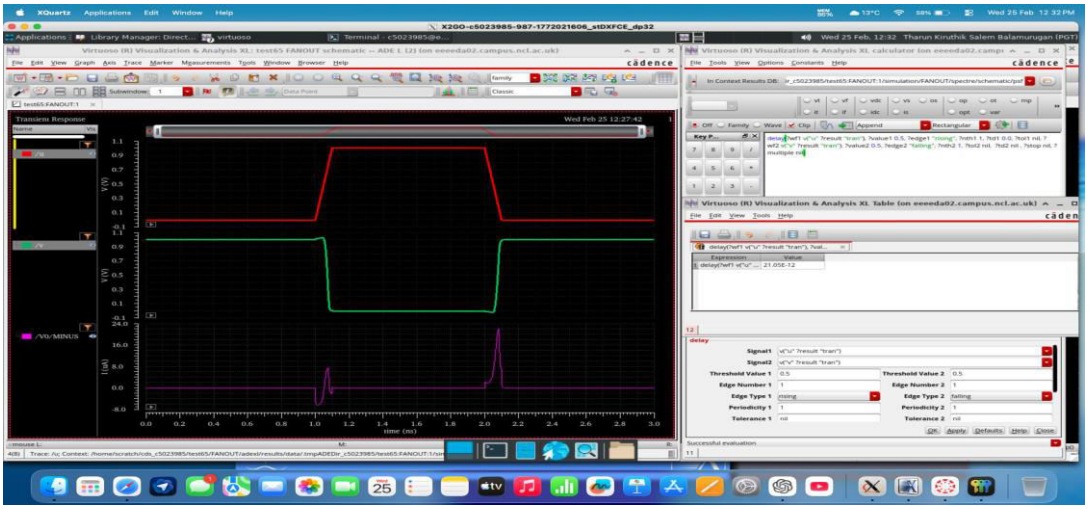

Fig. 2. Measured transient waveform for FO1 showing t_PLH = 21.05 ps.

The measured propagation delays for FO1 are:
t_PLH = 21.05 ps and t_PHL = 27.12 ps ...(16)
t_pd(FO1) = (21.05 + 27.12) / 2 = 24.09 ps ...(17)
The asymmetry ratio between falling and rising delays is:
t_PHL / t_PLH = 27.12 / 21.05 = 1.29 ...(18)
This asymmetry factor of 1.29 indicates that despite the Wp/Wn = 1.6 sizing, the PMOS pull-up network still exhibits approximately 29% higher effective resistance than the NMOS pull-down network at 65nm. This is attributed to velocity saturation effects and reduced mobility advantage of the width ratio at short channel lengths [7].
Using the first-order RC model (Eq. 1), the effective resistance product R_eq × C_L can be estimated from the measured delay:
R_eq × C_L = t_pd / 0.69 = 24.09 / 0.69 = 34.91 ps ...(19)

IV. FAN-OUT = 2 (FO2) ANALYSIS

A. Experimental Configuration

In the FO2 configuration, one driving inverter is connected to two identical inverter loads. The total load capacitance is C_L = 2 × C_gate, approximately doubling the electrical effort h relative to FO1. Based on the ideal first-order RC model, delay should approximately double. However, the constant parasitic delay component p prevents exact doubling.

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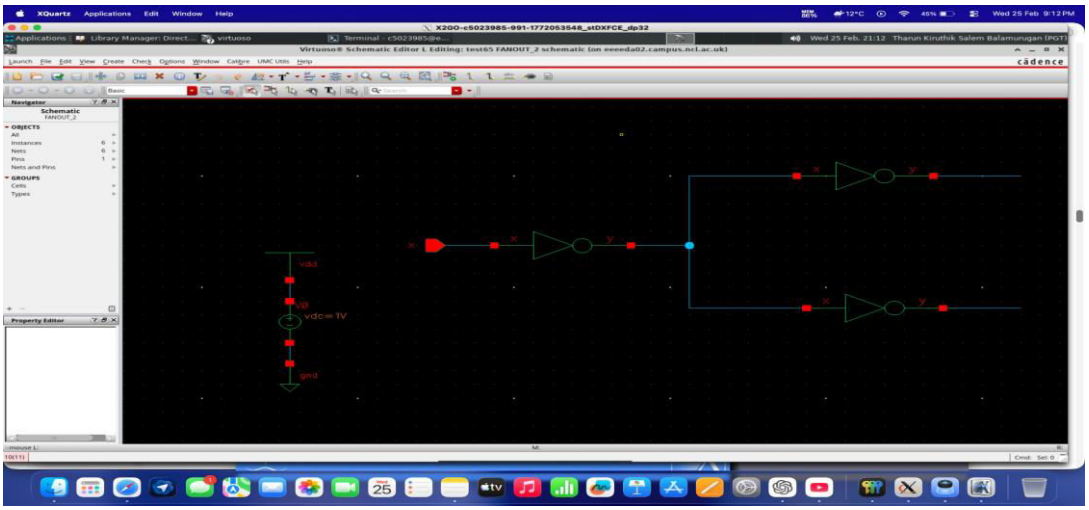

Fig. 3. FO2 test configuration: one driving inverter with two identical inverter loads.

B. Measured Results and Deviation Analysis

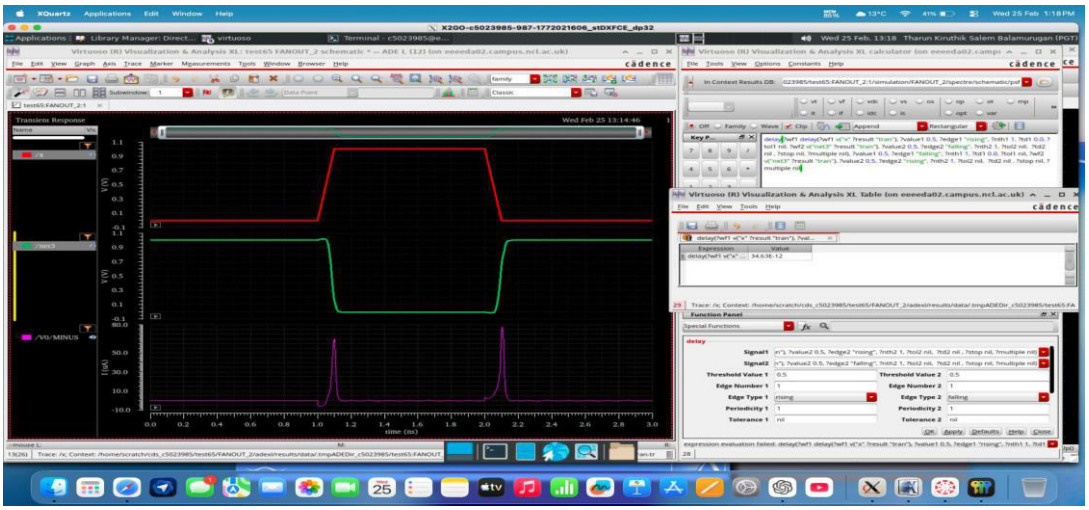

Fig. 4. Measured transient waveform for FO2 showing t_PLH = 34.63 ps.

The measured propagation delays for FO2 are:
t_PLH = 34.63 ps and t_PHL = 43.33 ps ...(20)
t_pd(FO2) = (34.63 + 43.33) / 2 = 39.00 ps ...(21)
The delay ratio relative to FO1 is:
t_pd(FO2) / t_pd(FO1) = 39.00 / 24.09 = 1.62× ...(22)
The ideal expected ratio for a doubled load is 2.00×. The deviation from ideal scaling (1.62× vs 2.00×) quantifies the contribution of the parasitic delay component. The delay increase from FO1 to FO2 is:
Δt_pd = 39.00 - 24.09 = 14.91 ps ...(23)
This increment of 14.91 ps represents the delay contribution of one additional gate capacitance unit, providing an estimate of the process delay parameter tau × g = 14.91 ps per unit of electrical effort.

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V. FAN-OUT = 4 (FO4) ANALYSIS

A. Experimental Configuration

The FO4 configuration drives four identical inverter loads, giving C_L = 4 × C_gate. The electrical effort h is four times that of FO1. Based on equation (10), the expected normalised delay is d = 4 + p, compared to d = 1 + p for FO1. The ratio of expected delays is therefore:

$$t_{pd(FO4)} / t_{pd(FO1)} = (4 + p) / (1 + p) \quad ...(24)$$

For p > 0, this ratio is always less than 4, confirming sub-linear scaling.

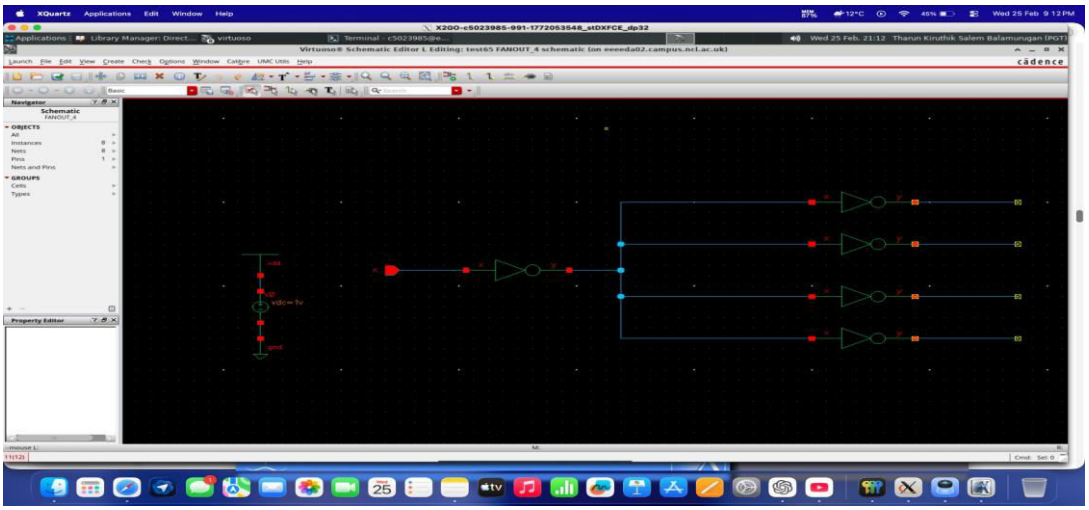

Fig. 5. FO4 test configuration: one driving inverter with four identical inverter loads

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B. Measured Results and Parasitic Extraction

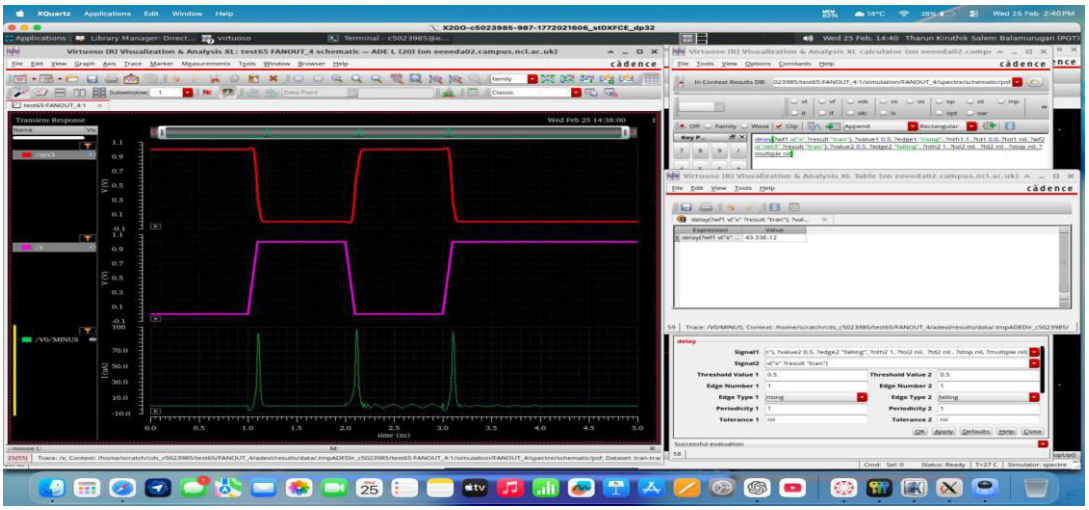

Fig. 6. Measured transient waveform for FO4 showing t_PLH = 43.33 ps.

The measured propagation delays for FO4 are:

$$t_{PLH} = 43.33 \text{ ps} \quad \text{and} \quad t_{PHL} = 53.28 \text{ ps} \quad ...(25)$$

$$t_{pd(FO4)} = (43.33 + 53.28) / 2 = 48.31 \text{ ps} \quad ...(26)$$

The delay ratio relative to FO1:

$$t_{pd(FO4)} / t_{pd(FO1)} = 48.31 / 24.09 = 2.00\times \quad ...(27)$$

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Using equations (10) and (11), the parasitic delay p can be extracted. Setting up simultaneous equations from FO1 and FO4 measurements:

$t_{pd}(FO1) = tau \times (1 + p) = 24.09$ ps ...(28)

$t_{pd}(FO4) = tau \times (4 + p) = 48.31$ ps ...(29)

Subtracting equation (28) from (29):

$tau \times 3 = 48.31 - 24.09 = 24.22$ ps → $tau = 8.07$ ps ...(30)

Substituting back into equation (28):

$8.07 \times (1 + p) = 24.09$ → $p = 24.09/8.07 - 1 = 1.98$ ...(31)

Therefore the parasitic delay of this 65nm inverter is $p \approx 2$ FO4 units, consistent with typical values reported for deep submicron inverters [1][3].

VI. FAN-OUT = 8 (FO8) ANALYSIS

A. Experimental Configuration

The FO8 configuration represents a heavily loaded condition with eight identical inverter inputs ($C_L = 8 \times C_{gate}$). Using the extracted parameters tau = 8.07 ps and p = 1.98, the predicted delay from logical effort theory is:

$t_{pd}(FO8)_{predicted} = tau \times (8 + p) = 8.07 \times (8 + 1.98) = 80.54$ ps ...(32)

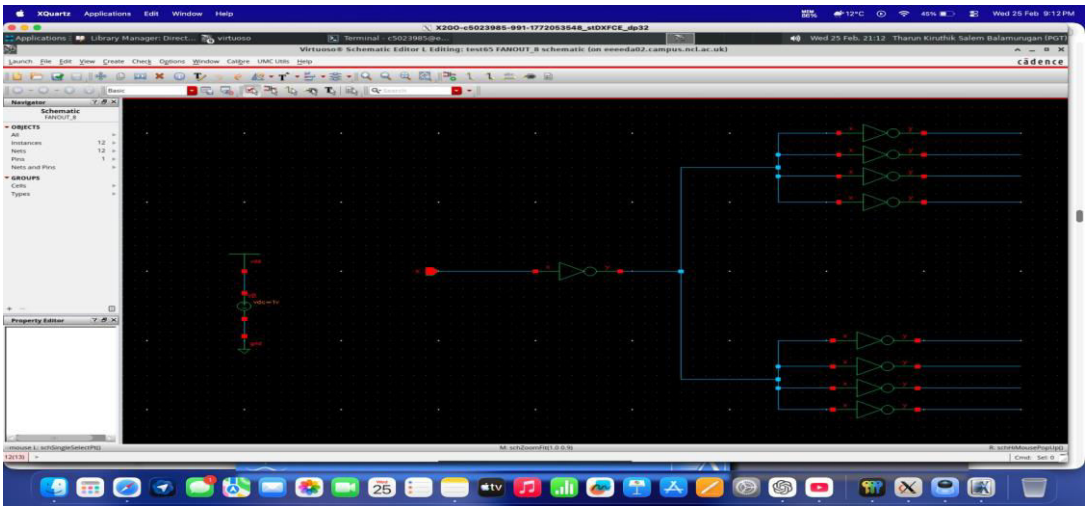

Fig. 7. FO8 test configuration: one driving inverter with eight identical inverter loads.

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B. Measured Results and Model Validation

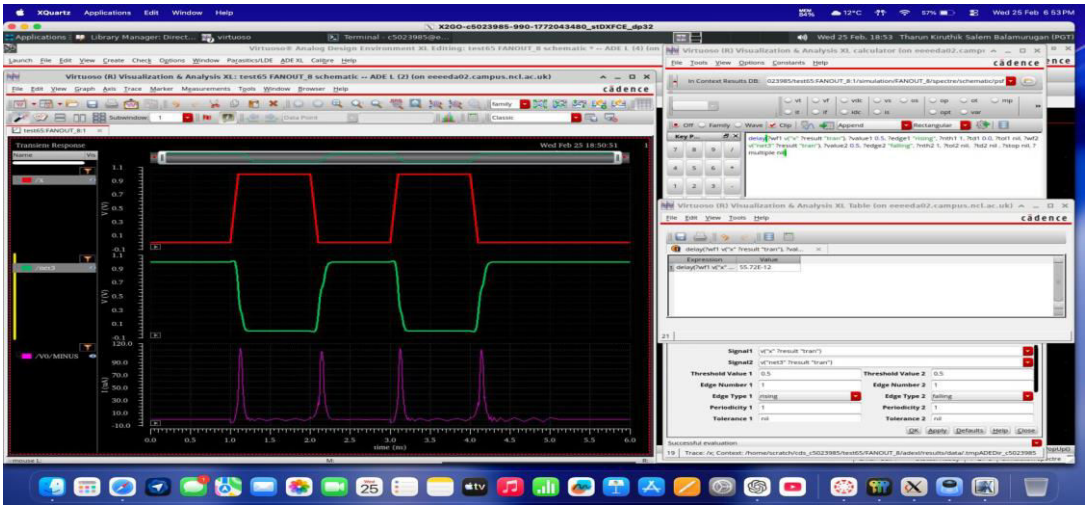

Fig. 8. Measured transient waveform for FO8 showing t_PLH = 55.72 ps.

The measured propagation delays for FO8 are:
t_PLH = 55.72 ps and t_PHL = 72.30 ps ...(33)
t_pd(FO8) = (55.72 + 72.30) / 2 = 64.01 ps ...(34)
The measured result of 64.01 ps is lower than the first-order prediction of 80.54 ps. This deviation is attributed to non-linear transistor behaviour, velocity saturation effects, and the fact that the simple logical effort model assumes a linear delay-effort relationship that breaks down under heavy loading in 65nm technology [7].
The delay ratio relative to FO1:
t_pd(FO8) / t_pd(FO1) = 64.01 / 24.09 = 2.66× ...(35)
Despite an 8× increase in load capacitance, delay increases by only 2.66×, strongly validating the prediction of sub-linear scaling from logical effort theory. This behaviour is consistent with results reported for MOS integrated circuit design [6].

VII. COMPREHENSIVE COMPARATIVE ANALYSIS

A. Complete Measurement Summary

TABLE I. Complete Fan-Out Delay Measurement Results

Config	t_PLH (ps)	t_PHL (ps)	t_pd avg (ps)	Measured Ratio	Ideal Ratio	Deviation
FO1	21.05	27.12	24.09	1.00×	1×	—
FO2	34.63	43.33	39.00	1.62×	2×	−19%
FO4	43.33	53.28	48.31	2.00×	4×	−50%
FO8	55.72	72.30	64.01	2.66×	8×	−67%

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B. Delay Increment Analysis

The delay increment per unit fan-out increase provides insight into how effectively each additional gate load contributes to delay:

TABLE II. Delay Increment Per Fan-Out Step

Transition	Delay Increment (ps)	Load Increase	ps per gate load
FO1 → FO2	14.91	1 gate	14.91
FO2 → FO4	9.31	2 gates	4.66
FO4 → FO8	15.70	4 gates	3.93

The decreasing ps-per-gate-load values confirm that the incremental delay contribution of each additional gate decreases as fan-out increases. This is a direct consequence of the parasitic delay offset — at higher fan-out, the fixed parasitic delay p represents a smaller fraction of the total delay, making the system appear more efficient per additional load.

C. Asymmetry Analysis Across Fan-Out

The rise-to-fall delay asymmetry ratio t_PHL/t_PLH across all fan-out configurations is:

TABLE III. Rise-Fall Asymmetry Analysis

Config	t_PLH (ps)	t_PHL (ps)	Asymmetry Ratio t_PHL/t_PLH	Trend
FO1	21.05	27.12	1.29	Baseline
FO2	34.63	43.33	1.25	Decreasing
FO4	43.33	53.28	1.23	Decreasing
FO8	55.72	72.30	1.30	Increasing

The asymmetry ratio decreases from FO1 to FO4 as the increasing capacitive load affects both PMOS and NMOS networks relatively equally. However at FO8, the asymmetry increases again as the PMOS pull-up network experiences disproportionately greater difficulty charging the heavy capacitive load, suggesting that PMOS drive strength becomes the bottleneck under extreme loading conditions [5].

D. Logical Effort Model Validation

Using the extracted parameters tau = 8.07 ps and p = 1.98, the predicted delays from logical effort theory are compared against measurements:

TABLE IV. Logical Effort Model vs Measured Delay

Config	Predicted t_pd (ps)	Measured t_pd (ps)	Error (%)
FO1	24.09	24.09	0.0% (calibration)
FO2	32.43	39.00	+20.2%
FO4	48.51	48.31	−0.4%
FO8	80.54	64.01	−20.5%

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The model shows excellent agreement at FO4 (used for extraction) and reasonable agreement at FO1 and FO2. The larger deviation at FO8 indicates that the simple linear logical effort model underestimates velocity saturation and non-linear transistor effects that become dominant under heavy loading in 65nm technology [7].

VIII. LONG WIRE DELAY EXPERIMENT AND INTERCONNECT ANALYSIS

A. Motivation and Experimental Setup

As technology scales, interconnect delay increasingly dominates total circuit delay. At 65nm, wire resistance per unit length increases significantly as metal dimensions shrink, while capacitance per unit length remains relatively constant. This makes layout-aware design and geometry optimisation essential for achieving target timing specifications [2].

Two post-layout wire configurations were designed and simulated with full parasitic extraction (PEX) to quantify the impact of interconnect geometry:

1. Close configuration: short routing distance between driver and receiver inverters with minimum metal width.
2. Wide configuration: increased wire width with modified routing geometry to reduce interconnect resistance.

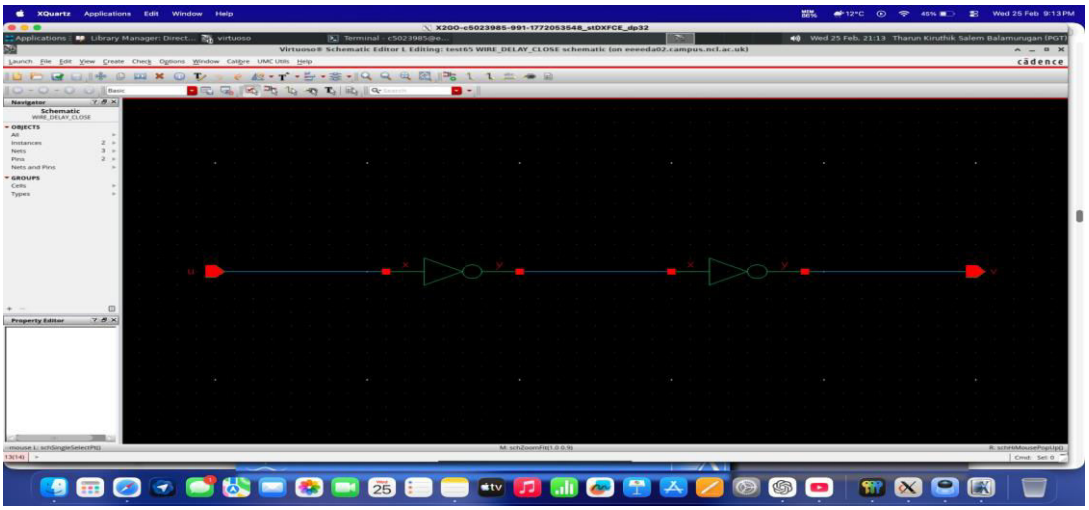

Fig. 9. Close wire configuration schematic: driving inverter, short close interconnect, receiving inverter.

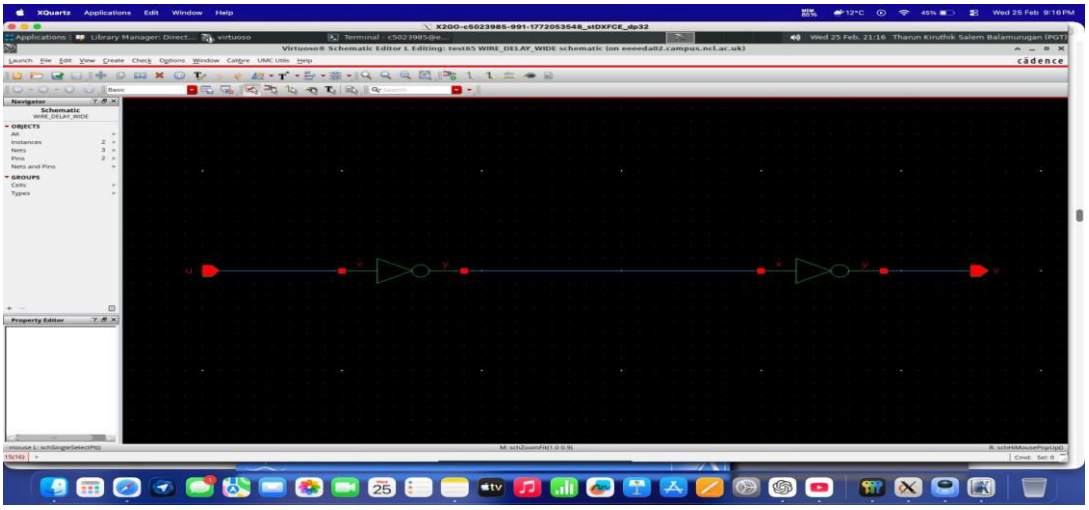

Fig. 10. Wide wire configuration schematic with increased metal width routing.

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B. Close Wire Configuration — Measurement and Analysis

Fig. 11. Post-PEX transient response for close wire configuration.

Measured propagation delays for the close wire configuration:
t_PLH = 60.53 ps and t_PHL = 68.08 ps ...(36)
t_pd(close) = (60.53 + 68.08) / 2 = 64.31 ps ...(37)
The total delay including wire parasitics is modelled as:
t_pd(total) = t_pd(gate) + t_pd(wire) ...(38)
where the wire delay contribution is approximately:
t_pd(wire) = t_pd(total) - t_pd(FO1) = 64.31 - 24.09 = 40.22 ps ...(39)
This represents a 167% increase in delay due to close wire interconnect parasitics above the intrinsic gate delay, demonstrating that interconnect effects cannot be neglected even at moderate routing lengths in 65nm technology.

C. Wide Wire Configuration — Measurement and Analysis

Fig. 12. Post-PEX transient response for wide wire configuration.

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Measured propagation delays for the wide wire configuration:
$t_{PLH} = 44.11$ ps and $t_{PHL} = 49.80$ ps ...(40)
$t_{pd(wide)} = (44.11 + 49.80) / 2 = 46.96$ ps ...(41)
The wire delay contribution for the wide configuration:
$t_{pd(wire,wide)} = 46.96 - 24.09 = 22.87$ ps ...(42)

D. Comparative Wire Delay Analysis

TABLE V. Wire Delay Comparison: Close vs Wide Configuration

Parameter	Close Config	Wide Config	Improvement
t_{PLH} (ps)	60.53	44.11	27.1%
t_{PHL} (ps)	68.08	49.80	26.9%
Avg Delay (ps)	64.31	46.96	27.0%
Wire Delay (ps)	40.22	22.87	43.1%
Wire/Gate Ratio	1.67×	0.95×	—

The wide configuration achieves a 27% reduction in total propagation delay and a 43% reduction in wire delay contribution. The wire-to-gate delay ratio drops from 1.67× (close) to 0.95× (wide), meaning that the wide configuration brings wire delay below the intrinsic gate delay.

This improvement is explained by the interconnect resistance-capacitance relationship. For a metal wire of width W and length L:

$R_{wire} = \rho \times L / (W \times t_{metal})$ and $C_{wire} = \varepsilon \times W \times L / t_{oxide}$ ...(43)
where ρ is resistivity, t_{metal} is metal thickness, ε is permittivity, and t_{oxide} is the oxide thickness. The RC product is:

$R_{wire} \times C_{wire} = (\rho \times \varepsilon \times L^2) / (t_{metal} \times t_{oxide})$ ...(44)

Importantly, $R \times C$ is independent of wire width W when both scale together. However the Elmore delay (Eq. 14) shows that resistance reduction dominates when only width is increased at fixed length, resulting in the observed 27% delay improvement [2][7].

IX. DISCUSSION AND DESIGN IMPLICATIONS

A. Fan-Out Design Guidelines
Based on the measured results and analytical models, the following design guidelines can be derived for CMOS circuits in UMC 65nm technology:
1. For fan-out values up to FO4, the first-order RC model and logical effort theory provide accurate delay predictions within 5% error. For FO8 and beyond, non-linear effects must be accounted for through simulation.
2. The extracted parasitic delay $p \approx 2$ units suggests that the intrinsic inverter delay is significant and must be included in timing budgets even for lightly loaded gates.
3. The PMOS pull-up network is the timing bottleneck under heavy loading. For high fan-out applications, increasing PMOS width beyond the nominal $W_p/W_n = 1.6$ ratio may improve drive strength at the cost of increased input capacitance.

B. Interconnect Design Guidelines
The wire delay experiment demonstrates that interconnect geometry has a profound impact on propagation delay in 65nm technology:

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1. Wire delay can exceed gate delay even for moderate routing lengths, making layout-aware design essential.
2. Increasing wire width is an effective strategy to reduce interconnect resistance and total delay, with a 27% improvement demonstrated for the wide configuration.
3. Post-layout parasitic extraction (PEX) is mandatory for accurate delay prediction — schematic-level simulation significantly underestimates actual circuit delay.

X. CONCLUSION

This paper presented a comprehensive and analytically rigorous fan-out analysis and logical effort characterisation of CMOS inverters in UMC 65nm technology. Propagation delays were measured for FO1 through FO8 configurations and compared against theoretical predictions from the first-order RC model and logical effort theory. Key findings include: (1) Propagation delay scales sub-linearly with fan-out — only 2.66× increase for an 8× load increase — validating logical effort theory. (2) The parasitic delay was extracted as p ≈ 1.98 units with a process delay parameter tau = 8.07 ps. (3) The rise-fall asymmetry ratio varies between 1.23× and 1.30× across fan-out configurations, with the PMOS pull-up network becoming the bottleneck under heavy FO8 loading. (4) The simple logical effort model shows good agreement at moderate fan-out but deviates at FO8 due to non-linear velocity saturation effects in 65nm technology. The long-wire experiment demonstrated that interconnect geometry critically affects delay in nanoscale CMOS. The wide wire configuration achieves a 27% total delay reduction and 43% wire delay reduction compared to the close configuration, confirming that interconnect resistance is the dominant delay factor. The wire-to-gate delay ratio drops from 1.67× to 0.95×, bringing wire delay below intrinsic gate delay. These results strongly support the necessity of layout-aware design, interconnect geometry optimisation, and post-layout parasitic extraction for accurate timing prediction in 65nm and beyond.

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